REMARKS

Claims 1-15 are pending in this application. Claims 1, 8 and 15 are amended. No new matter has been added. Applicant respectfully requests reconsideration of the claims in view of the following remarks.

The amendment to claim 1 finds support at least from original claim 1, page 5 line 1 to line 2 and Figure 3. The amendment to claim 15 finds support at least from original claim 15 and page 6 line 17 to page 7 line 5 and Figure 6.

Claim 15 has been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claim 15 has now been amended to make it clear the second memory is "directly coupled to the system bus" unlike the first memory which is coupled through an interface according to claim 1.

Claims 1, 3-6 and 8-13 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Merrell, *et al.* (U.S. Patent No. 5,829,038, hereinafter "Merrell"). Applicant respectfully traverses this rejection.

The Examiner considers Merrell to disclose or teach all of the features of claims 1, 3-6 and 8-13 of the present application. Applicant submits that each and every element as set forth in the claims 1, 3-6 and 8-13 is not found, either expressly or inherently, in Merrell. Thus, the cited reference does not anticipate the claimed invention.

The present invention as now defined in independent claim 1, which requires:

> A data processing system having:
> at least one processor chip including a processor unit and an internal data cache, and
> an interface configured to receive data from the processor chip, the interface further configured to discard all the data to be written to an external memory received from the processor chip.

and claim 8, which requires:

> A data processing system comprising:
> a processor chip including an internal processor coupled to an internal data cache;

an external memory; and

an interface coupled between the processor chip and the external memory, the interface configured to receive memory data from the external memory and transfer the memory data to the processor chip, the interface further configured to receive processor data from the processor chip and discard all the processor data to be written to the external memory.

The present invention relates to an improved method of using a standard processor chip, and to a data processing system including a standard data processing chip making use of this improved method.

A standard data processing chip includes a processor unit and an internal data cache. Such a chip will also generally provide a device controller for controlling the flow of data to and from an external memory and the internal data cache. As described in the present application, data to be stored in memory is written from the processor chip to an external memory, generally via an interface. This writing of data to an external memory, and the retrieval of information from this external memory, can be slow, and therefore reduces the operating speed of the device.

A possible solution to this problem would be to use a different processor chip that does not write data to an external memory. However, the use of a dedicated chip with this functionality may be costly, especially since this would require the design of different chips, and the manufacture of different chips depending upon the intended use, namely whether they are to export data to an external memory or not.

According to the present invention, the solution is to use a standard processor chip, in which data is transmitted from the processor chip. However, this transmitted data is not actually written to external memory, but discarded. Accordingly, the delays associated with writing the data to an external memory are avoided. Further, since the data is not written to an external memory, the data is only stored in the internal cache of the processor chip. When the data is read, it is read from the internal cache which can be read at a faster rate than would be the case

from an external memory. Accordingly, this again improves the speed of the device. Nevertheless, since the data is still exported from the processor chip itself, there is no need to modify the operation of the processor chip, or to use a different processor chip. Accordingly, the disadvantages that would be associated with providing a different processor chip are avoided.

Merrell instead discloses the normal operation which is common in the prior art, wherein under normal circumstances, data is transferred between the CPU and the cache and the external memory as and where required. Clearly, in Merrell, the question is not whether data is discarded from the cache as suggested by the Examiner. Instead, the question is, whether data is sent from the processor and the cache with the intention of being written to an external memory, which is in turned received by an interface external to the processor and the cache which then discards all of the received data. Even if, in the case of Merrell, the program being run is only as big as the cache, the disclosure still does not anticipate the requirements of claim 1.

Clearly, Merrell does not disclose any interface between the processor/cache and the external memory. The hierarchical cache structure 15 of Merrell is integral to the cache and is not a separate external component. There is no discarding of data once it leaves the cache on its way to the external memory. The problem to be solved by the present invention is not identified or even suggested in Merrell. In Figure 1, there are clearly no interfaces between the cache 15 and the memory 60. Clearly, there is no possibility of discarding of data between the cache and the memory. Therefore, Merrell is not relevant to the invention of claim 1.

The required elements of currently amended claims 1 and 8 are not found in Merrell. Accordingly, Applicant submits that currently amended claims 1 and 8 are not anticipated by Merrell.

Claims 3-6 and 9-13 add further limitations to claims 1 and 8. Merrell does not anticipate claims 1 and 8 for the reasons given above, and these reasons are repeated in relation to the patentability of claims 3-6 and 9-13. Applicant submits that claims 3-6 and 9-13 are not anticipated by Merrell, by reason of depending from an allowable claim as well for adding further new limitations not found in Merrell.

For example, claim 3 requires that the data processing system includes at least one further processing chip. In accordance with this claim, there will be a total of at least two processor chips, namely that of claim 1, and the additional chip of claim 3. The claim further requires that the additional processing chip has read/write access to an external memory. This is in accordance with the conventional arrangement of processing chips where the processing chip has read and/or a write access to external memory. Accordingly, claim 3 covers an arrangement having two or more processor chips, one processor having no access to external memory in accordance with the main embodiment of the present invention, another processor having access to an external memory. This may be appropriate were one processor requires a larger memory store, and must therefore write to an external memory, irrespective of the speed disadvantages that are overcome with the present invention. In other words, there are some instances where the advantages of the method of the present invention are outweighed by other considerations, such as storage capacity, and in these circumstances the use of an external memory in a conventional manner may be advantageous. There will be cases where two processor chips may be used, one functioning in accordance with the present invention with no ability to write to an external memory, and another being able to act in a conventional manner.

Applicant submits claim 3 is also patentable over Merrell.

To establish a *prima facie* case of obviousness, three basic criteria must be met (M.P.E.P. § 2143). First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to an artisan of ordinary skill in the art, as of the date of invention, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references when combined must teach or suggest all of the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable chance of success must both be found in the prior art, not in the Applicant's disclosure. *In re Vaeck,* 947 F.2d 488,20 USPQ2d 1438 (Fed. Cir. 1991)

Claims 2 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Merrell in view of Klein (US Patent No. 6,401,199, hereinafter "Klein"). More specifically, the Examiner has objected to dependent claim 2 as he considers this claim to be obvious in light of a combination of the teachings of Merrell and Klein.

The Examiner admits Merrell does not disclose "passing data to the processor chip during initialization". The Examiner goes on to state "it would have been obvious…to have the processor chip initialize through the cache hierarchy interface of Merrell, because Klein teaches that running bootstrap programs from RAM instead of ROM is faster.

To the contrary, claim 2 does not suggest switching initialization from ROM to RAM. Klein is not relevant to claim 2.

Furthermore, the comments above in relation to the novelty of currently amended claim 1 are reiterated in relation to the non obviousness of previously presented claim 2. Klein does not provide any of the features previously indicated as lacking in Merrell. Klein does not disclose an

interface external to the processor/cache, which discards all data to be written to external memory as defined in claim 2.

In view of the above, it is also clear that one of ordinary skill in the art would not even consider it obvious to try the alleged combination, let alone the required standard of a reasonable expectation of success.

The required elements of previously presented claim 2 are not found in Merrell, Klein or any valid combination thereof. Accordingly, Applicant submits that previously presented claim 2 is non obvious over Merrell in view of Klein.

Claims 7 and 10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Merrell in view of "The Cache Memory Book" by Jim Handy (hereinafter "Handy"). More specifically, the Examiner has objected to dependent claims 7 and 10 as he considers these claims to be obvious in light of a combination of the teachings of Merrell and Handy.

The Examiner admits that Merrell does not disclose "an internal cache controller coupled between the internal data cache and the processor unit". The Examiner also states "it would have been obvious…to have the cache controller between the internal data cache and processor unit in the system of Merrell et al., because Handy teaches that all CPU/cache interactions are controlled by the cache controller which must intercept all of the CPU's signals, therefore it would be obvious for the cache controller to be between the internal data cache and processor unit."

However, the statement by the Examiner does not indicate why this combination/modification would be desirable.

Hence the combination is not valid for claim 7.

The Examiner admits that Merrell does not disclose "the control circuit comprises a decoder". The Examiner also states "it would have been obvious…to have a decoder in the control circuit of Merrell et al., because Handy teaches that using a decoder with the control circuit for the cache reduces delays in determining cache hits and misses".

However, the present invention in claim 10 requires that a control circuit provide a control signal to the interface circuit where the control circuit is a decoder. Therefore the decoder with the control circuit does not control the internal cache as suggested by the Examiner.

Hence, the combination is not valid for claim 10.

In any case, the comments above in relation to the novelty of currently amended claims 1 and 8 are reiterated in relation to the non obviousness of previously presented claims 7 and 10. Thus Handy does not provide any of the features previously indicated as lacking in Merrell. Handy does not disclose an interface external to the processor/cache which discards all data to be written to external memory as defined in claims 7 and 10.

In view of the above, it is also clear that one of ordinary skill in the art would not even consider it obvious to try the alleged combination, let alone the required standard of a reasonable expectation of success.

The required elements of previously presented claims 7 and 10 are not found in Merrell, Handy or any valid combination thereof. Accordingly, Applicant submits that previously presented claims 7 and 10 is non obvious over Merrell in view of Handy.

Claims 14 and 15 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Merrell in view of Stewart, *et al.* (US Patent No. 5,157,780, hereinafter "Stewart"). More specifically, the Examiner has objected to dependent claims 14 and 15 as he considers these claims to be obvious in light of a combination of the teachings of Merrell and Stewart.

The Examiner admits that the Merrell does not disclose "the third processor chip comprises a master processing unit and wherein the processor chip and the second processor chip comprise slave processing units". The Examiner also states that "it would have been obvious...to have a plurality of processors implemented in a master/slave configuration in the system of Merrell et al., because Stewart et al. teaches that it is common to use redundant processors to provide a fail-safe mode of operation".

The Examiner seems to be suggesting that the processor chip and the second processor chip are redundant and can be used to provide a fail-safe mode of operation. However, this is not relevant to the present invention in claim 14 since there was no requirement of redundancy.

Hence the combination is not valid for claim 14.

It is not clear whether or not the Examiner admits that Merrell does not disclose "a second external memory coupled to the system bus without an interface coupled between the second external memory and the system bus". However, presuming that the Examiner is admitting this, the Examiner also states that "it would have been obvious...to have a second external memory coupled to the system bus in the system of Merrell et al., because it is notoriously well-known and common in the art to have a hard disk supplying data to the volatile main memory".

Since claim 15 now requires that the second external memory is directly connected to the system bus, this rejection is moot. In any event, the comments above in relation to the novelty of currently amended claims 1 and 8 are reiterated in relation to the non obviousness of previously presented claims 14 and 15. Stewart does not provide any of the features previously indicated as lacking in Merrell. Stewart does not disclose an interface external to the processor/cache that discards all data to be written to external memory as defined in claims 14 and 15.

In view of the above, it is also clear that one of ordinary skill in the art would not even consider it obvious to try the alleged combination, let alone the required standard of a reasonable expectation of success.

The required elements of previously presented claims 14 and 15 are not found in Merrell, Stewart or any valid combination thereof. Accordingly, Applicant submits that previously presented claims 14 and 15 are non obvious over Merrell in view of Stewart.

It is felt that a full and complete response has been made to the Office Action, and Applicant respectfully submits that the pending claims are allowable over the cited art and that subject application is now in condition for allowance.

The fact that Applicant may not have specifically traversed any particular assertion by the Office should not be construed as indicating Applicant's agreement therewith.

Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Ira S. Matsil, Applicant's attorney, at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge Deposit Account No. 50-1065.

Respectfully submitted,

June 20, 2007
Date

/Ira S. Matsil/
Ira S. Matsil
Attorney for Applicant
Reg. No. 35,272

SLATER & MATSIL, L.L.P.
17950 Preston Rd., Suite 1000
Dallas, Texas 75252
Tel.: 972-732-1001
Fax: 972-732-9218